(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 584 627 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **93112765.8**

(51) Int. Cl.5: **H04J 3/16**

(22) Date of filing: **10.08.93**

(30) Priority: **25.08.92 US 935008**

(43) Date of publication of application:
02.03.94 Bulletin 94/09

(84) Designated Contracting States:
AT BE CH DE ES FR GB IT LI NL SE

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(54) Incremental phase smoothing desynchronizer and calculation apparatus.

(57) A desynchronizer (20) for desynchronizing data stored within synchronous payload envelopes of a synchronous communication protocol such as SONET (Synchronous Optical Network), provides for smoothing the periodically discontinuous clock signal associated with that data after the synchronous communication protocol overhead has been removed. The desynchronizer accommodates for shifts in the position of the payload envelope and hence, the data within the synchronous communication frame as well as adjustments within the data itself due to asynchronous bit stuff information. The desynchronizer utilizes a leak filter (26) having a linear branch (54) and an integrator branch (56), both branches having adjustable factors (61, 63, 65, 88, 90, 91, 93, 95, 100, 102, 105) regarding their operation, wherein the adjustable factors are selected depending upon threshold values (86, 87, 89, 62) which in turn are based upon the difference between the average write address and read address for the associated elastic store (22) within which the incoming data removed from the synchronous communication system frame is temporarily stored. The leak filter (26) forms part of a phase locked loop which in turn adjusts the read clock frequency (46) in a manner which minimizes overflow or underflow of the elastic store while simultaneously minimizing the rate of change of the read clock rate so as to limit jitter. A fault recovery apparatus forms part of the desynchronizer for enabling fastlock high gain factors (67, 97, 107) to quickly adjust the read clock when elastic store overflow or underflow occurs. The gain factor associated with both the linear branch and integrator branch are provisionable (118, 120) as well as elastic store size and thresholds resulting in a desynchronizer which can be modified to meet the particular jitter requirements of a particular synchronous communication system. A calculation engine (82) performs iterative calculations to generate the leak filter output value using a reduced number of logic gates for ASIC implementation.

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